CMOS beyond Si:
Nanometer-Scale III-V MOSFETs

J. A. del Alamo, X. Cai, J. Lin, W. Lu, A. Vardi, and X. Zhao

Microsystems Technology Laboratories
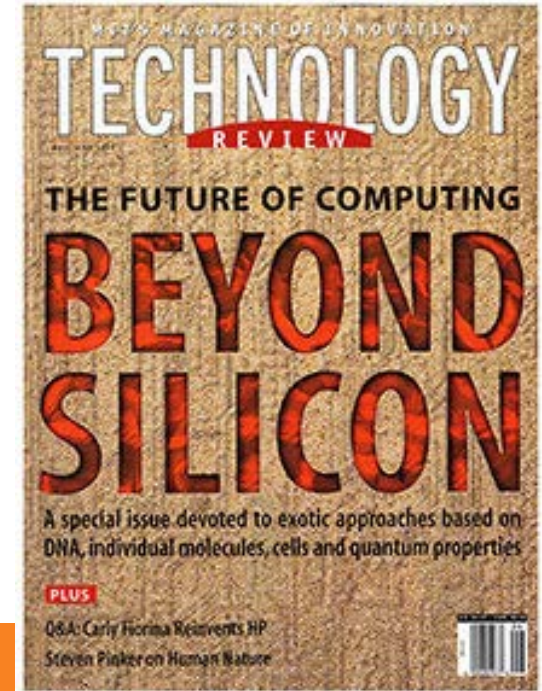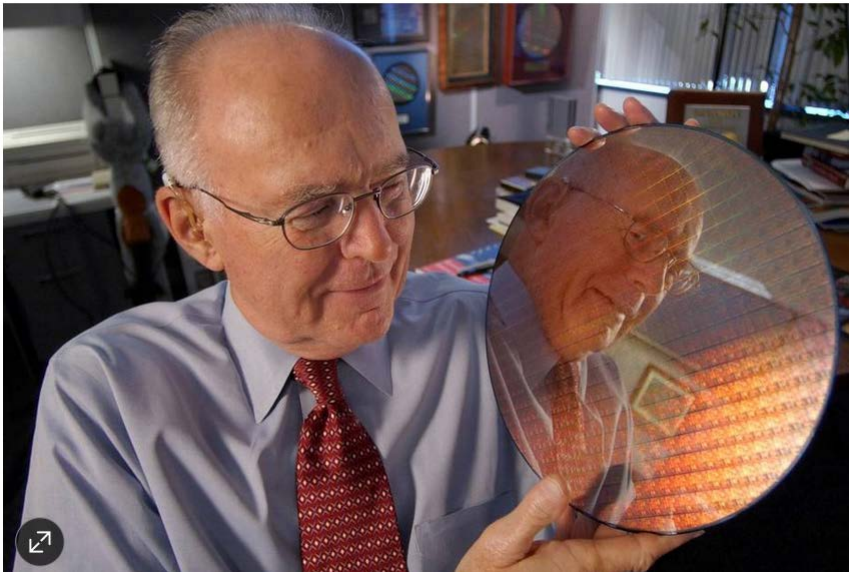
Massachusetts Institute of Technology

Moore's Law at 50: the end in sight?

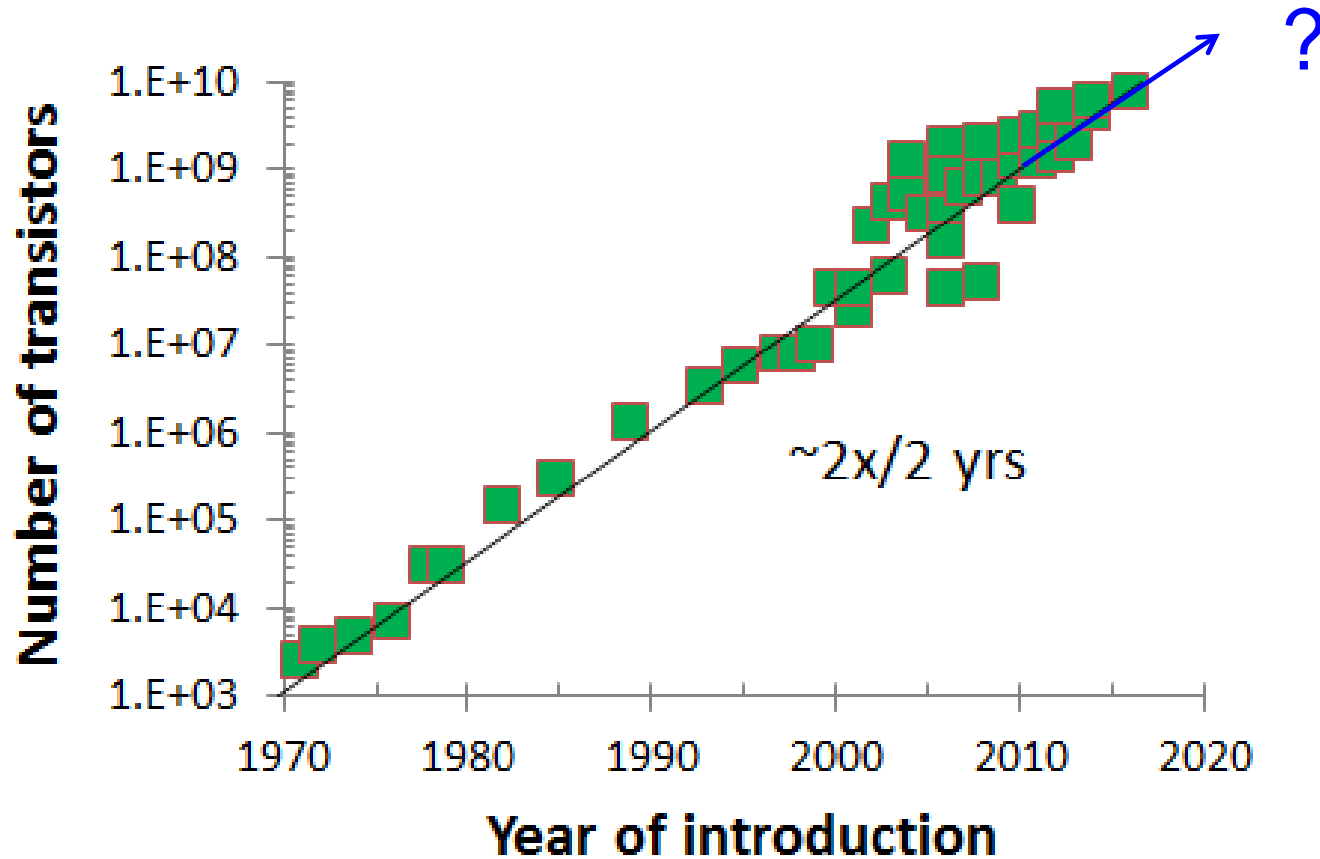THE WALL STREET JOURNAL.

Moore's Law Is Showing Its Age

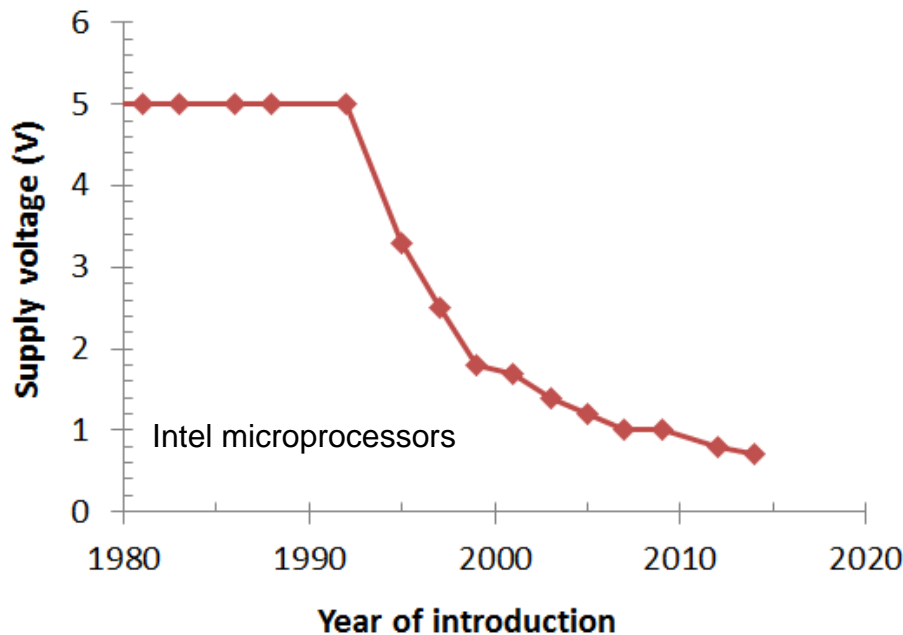The prediction about squeezing transistors onto silicon has been revised again.

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Moore's Law
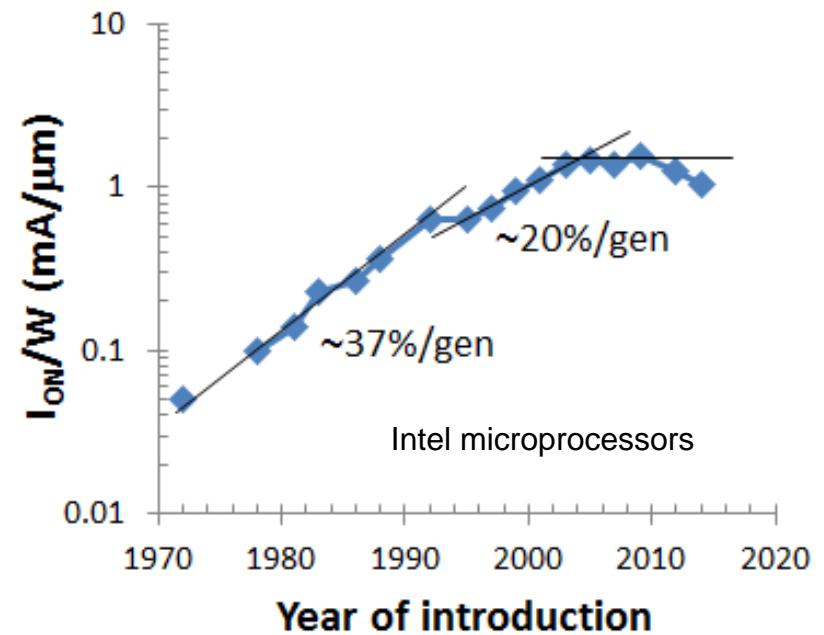
How far can Si support Moore's Law?

The problem:

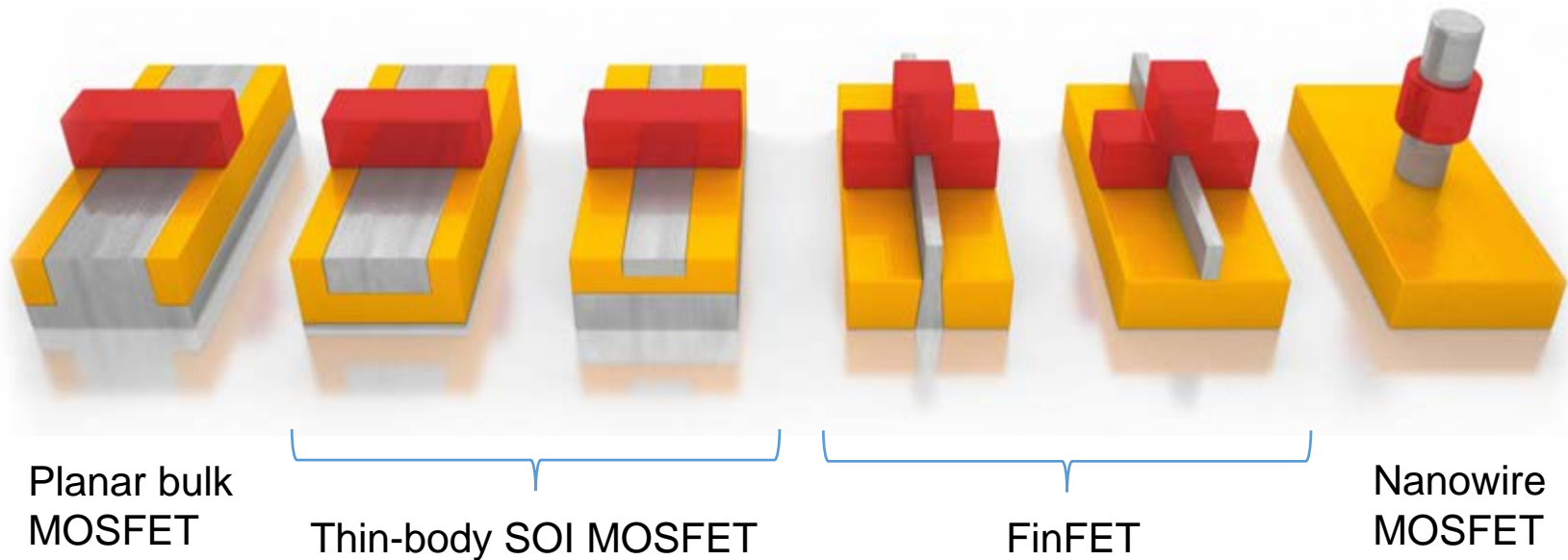## Transistor scaling → Voltage scaling → Performance suffers

Supply voltage: Transistor current density:

Intel microprocessors   ~20%/gen

~37%/gen

Intel microprocessors

What can we do about this?

Moore's Law:
it's all about MOSFET scaling

1. New device structures with improved scalability:

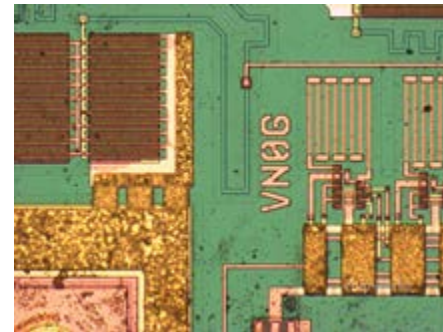Planar bulk MOSFET   Thin-body SOI MOSFET   FinFET   Nanowire MOSFET
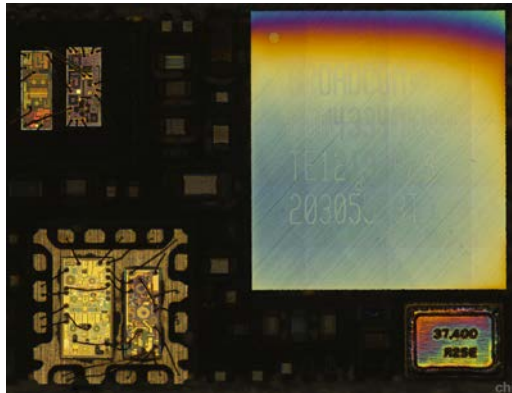
2. New materials with improved transport characteristics:

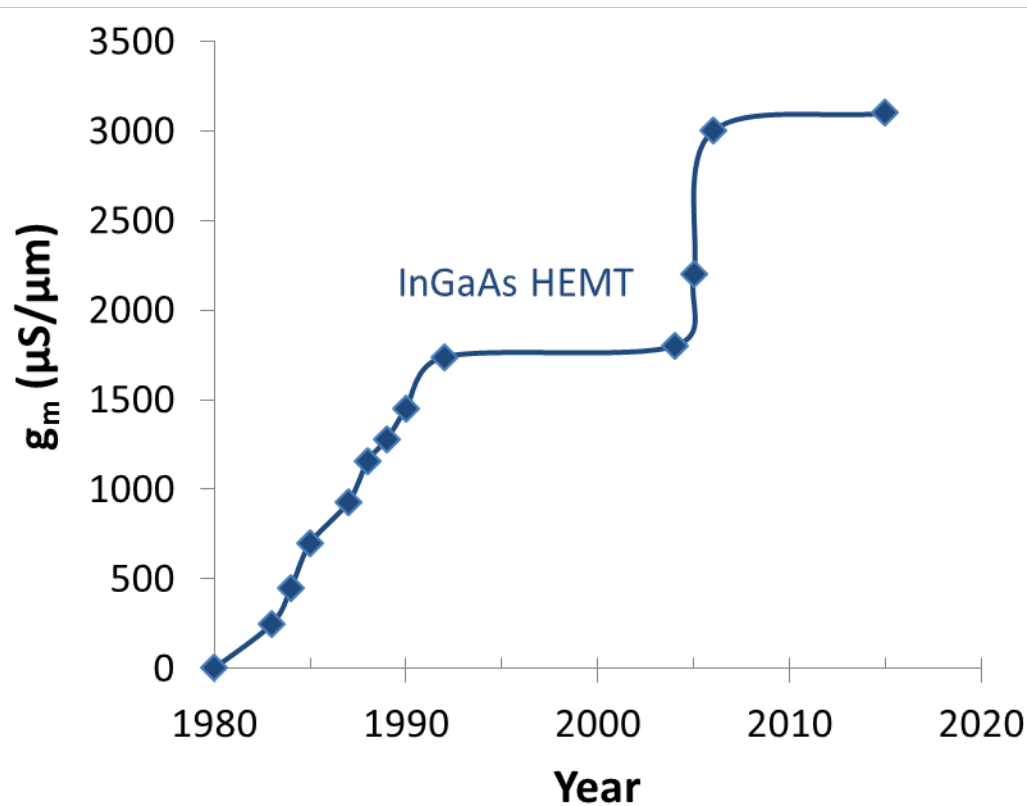n-channel: Si → Strained Si → SiGe → InGaAs

p-channel: Si → Strained Si → SiGe → Ge → InGaSb

III-V electronics in your pocket!

Transconductance ($g_m = dI_D/dV_{GS}$):
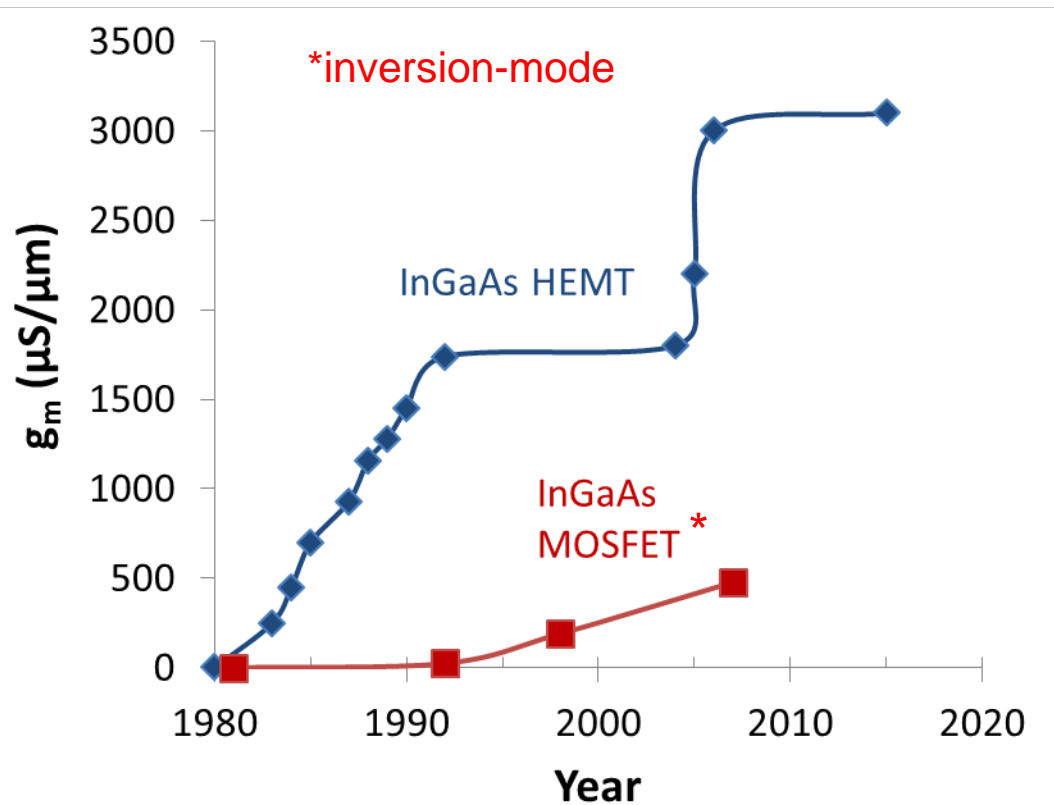

InGaAs channel

InAlAs barrier

InGaAs HEMT

InGaAs MOSFETs vs. HEMTs

Transconductance ($g_m = dI_D/dV_{GS}$):

*inversion-mode

InGaAs HEMT

InGaAs MOSFET *

InGaAs channel

InAlAs barrier

InGaAs channel

High-K oxide

InGaAs MOSFETs vs. HEMTs

Transconductance ($g_m = dI_D/dV_{GS}$):

*inversion-mode

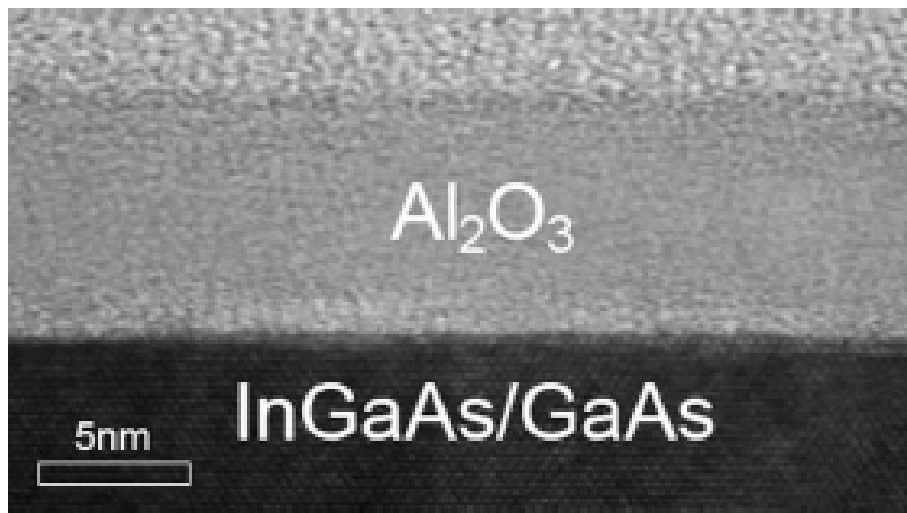g_m=3.45 mS/µm
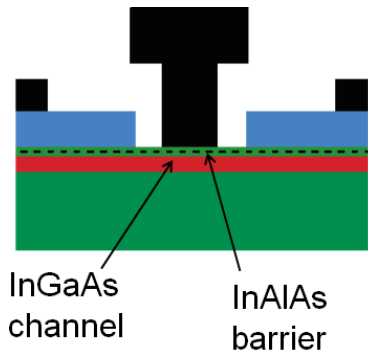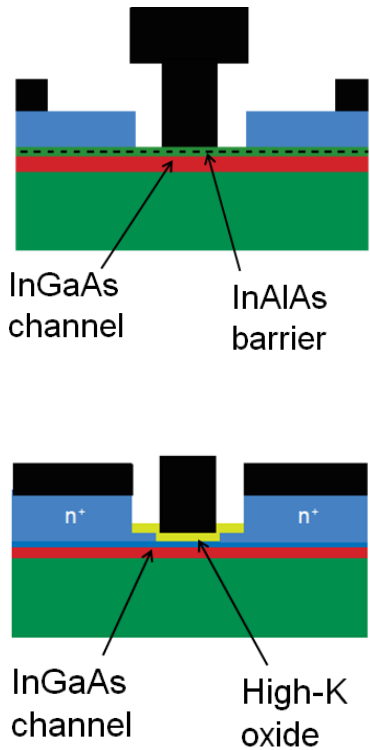
InGaAs HEMT

InGaAs MOSFET *
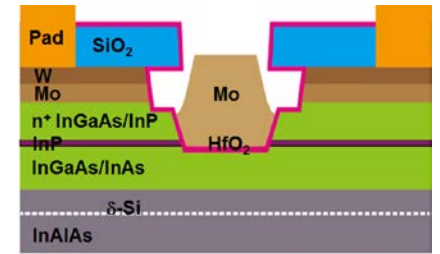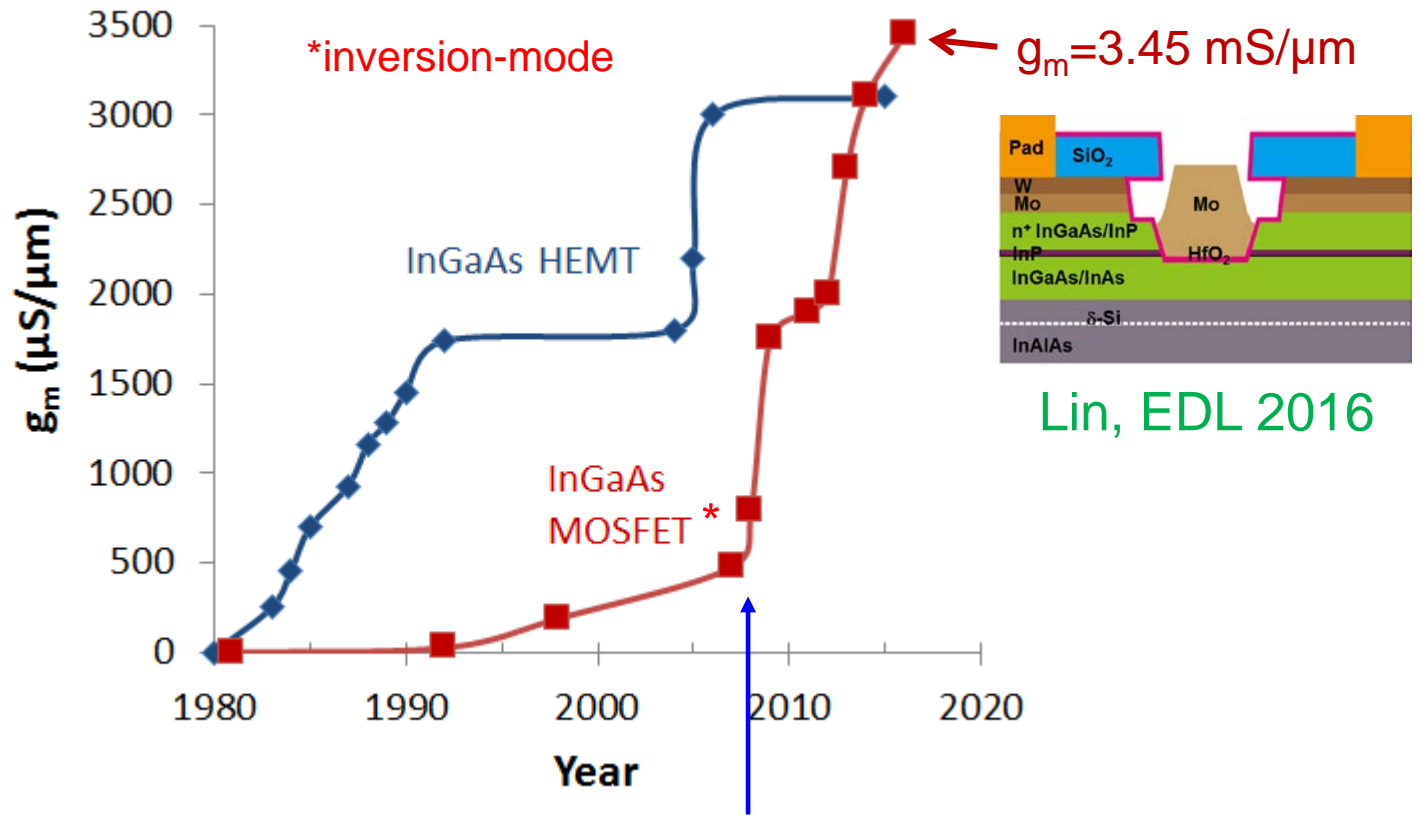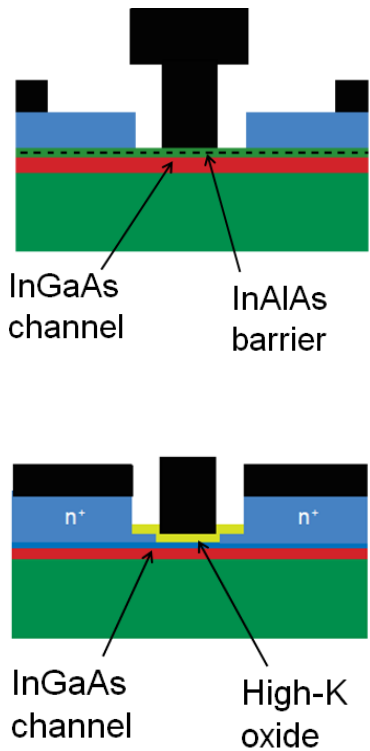
Lin, EDL 2016

What happened here?

Atomic Layer Deposition (ALD) of gate oxide

ALD eliminates residual native oxides that pin Fermi level

→ "Self cleaning"

Huang, APL 2005

Clean, smooth ← interface without native oxides

Al_2O_3

5nm

InGaAs/GaAs

- First with Al_2O_3, then with other high-K dielectrics
- First in GaAs, then in other III-Vs

Planar Si and InGaAs MOSFET Benchmark

n-MOSFETs in Intel's nodes at nominal voltage
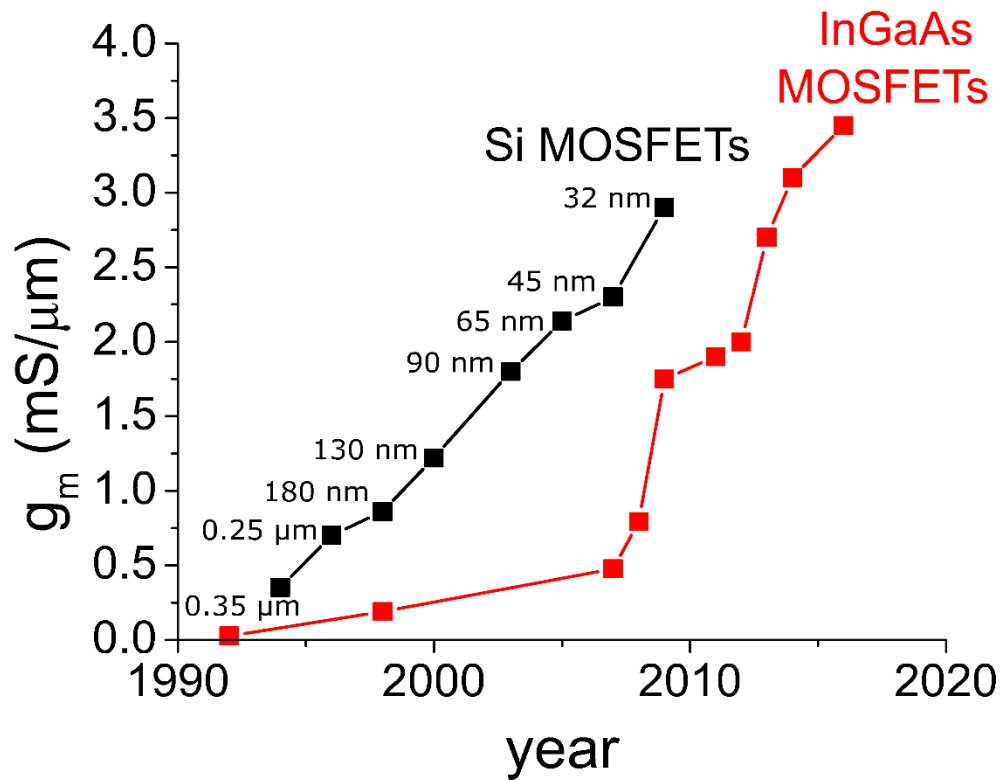
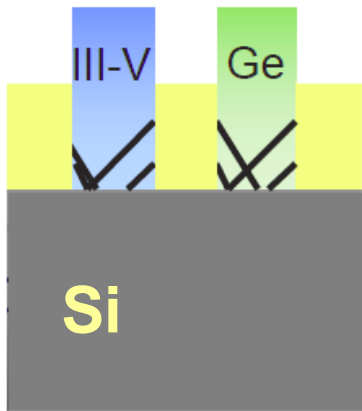Comparisons always fraught with danger…

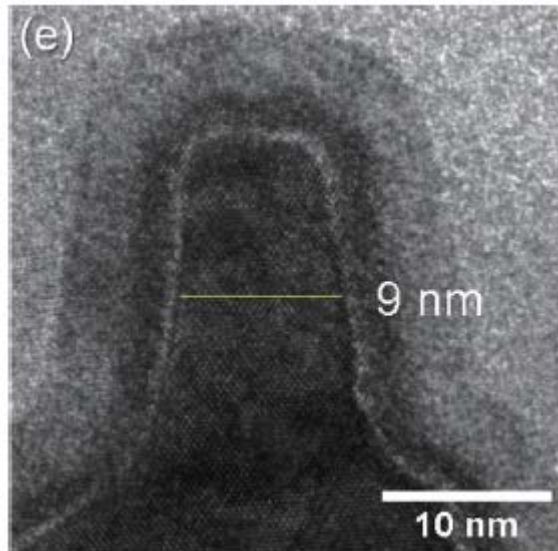Transconductance exceeds Si MOSFETs

InGaAs FinFETs

FinFETs

Bottom-up InGaAs FinFETs

Aspect-Ratio Trapping
Fiorenza, ECST 2010

Epi-grown fin inside trench

9 nm

10 nm
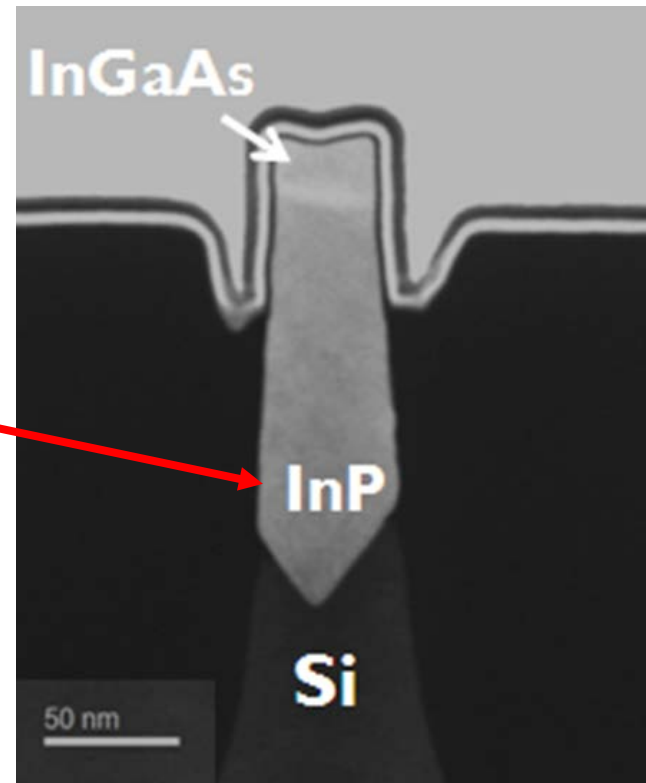
Sun, VLSI Tech 2017

Waldron, VLSI Tech 2014

InGaAs FinFETs @ MIT
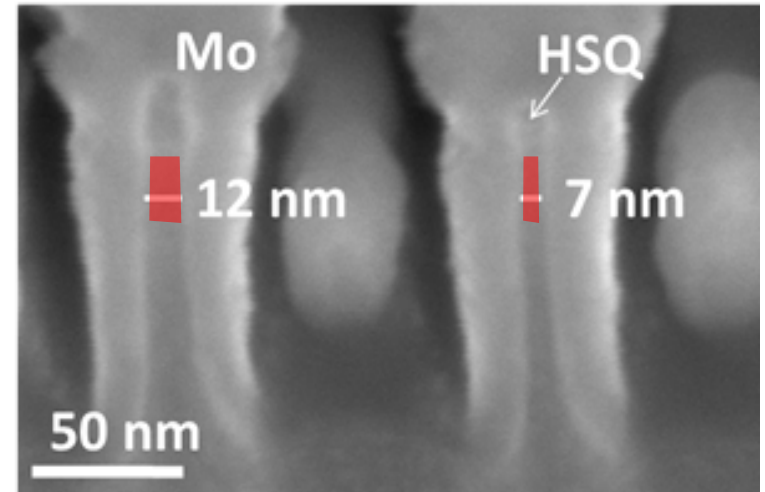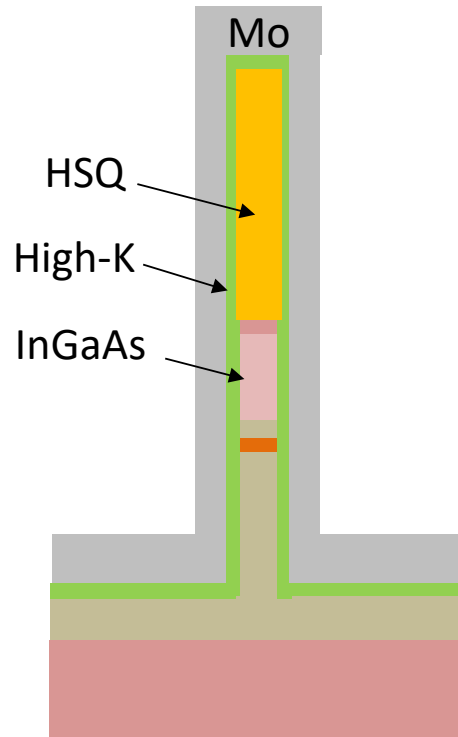
Key enabling technologies: $BCl_3/SiCl_4/Ar$ RIE + digital etch
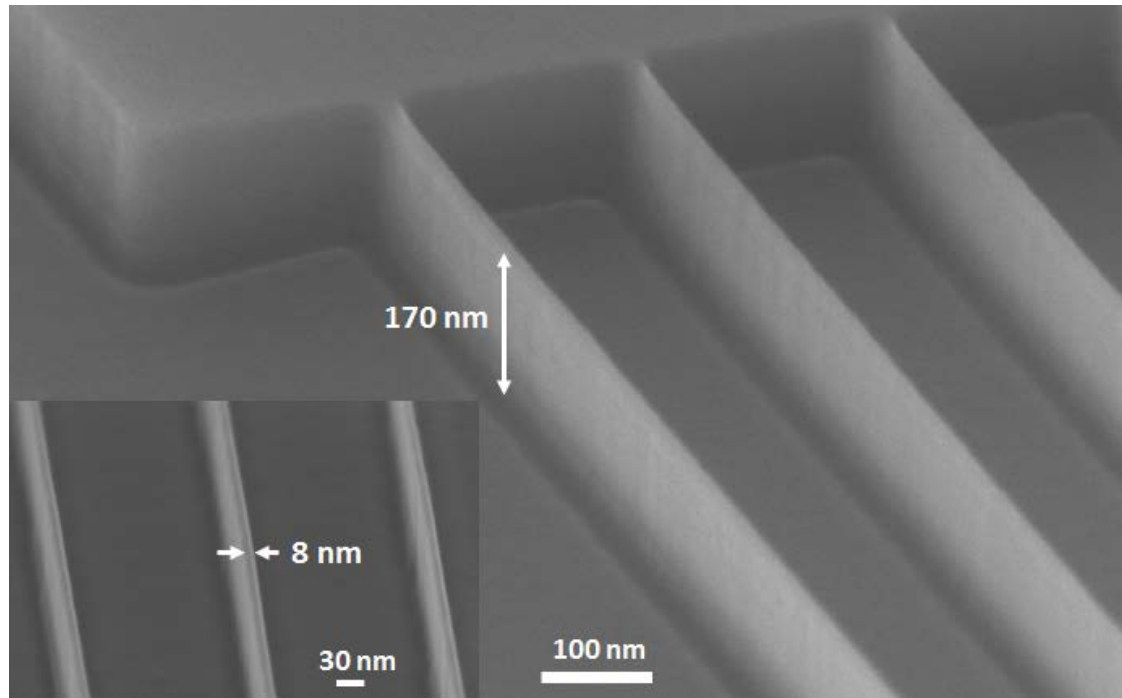
- Sub-10 nm fin width
- Aspect ratio > 20
- Vertical sidewalls

Vardi,
DRC 2014,
EDL 2015,
IEDM 2015

InGaAs FinFETs @ MIT

- **Si-compatible process**
- **Contact-first, gate-last process**
- **Fin etch mask left in place → double-gate MOSFET**
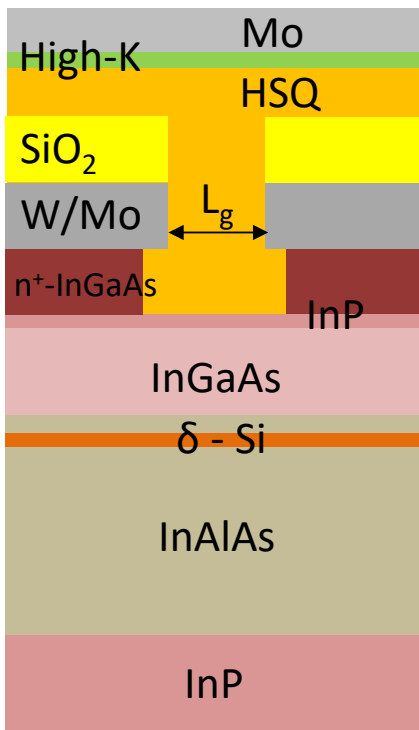
Vardi, VLSI Tech 2016

Vardi, EDL 2016

Most aggressively scaled FinFET

W_f=7 nm, L_g=30 nm, H_c=40 nm (AR=5.7), EOT=0.6 nm:
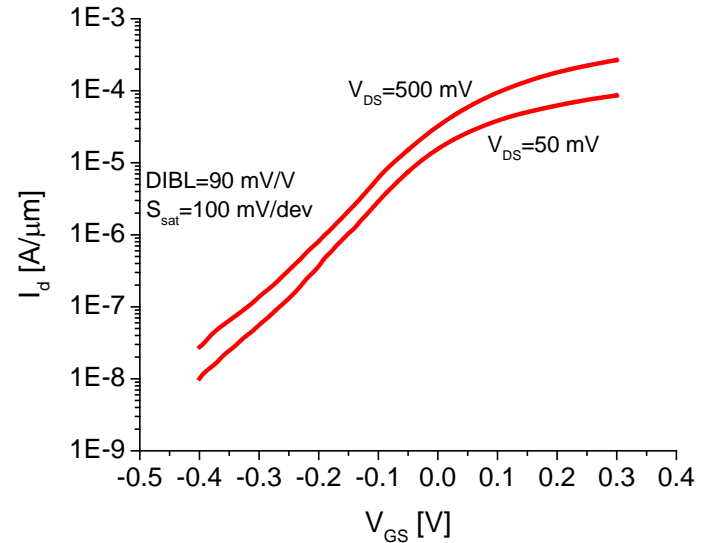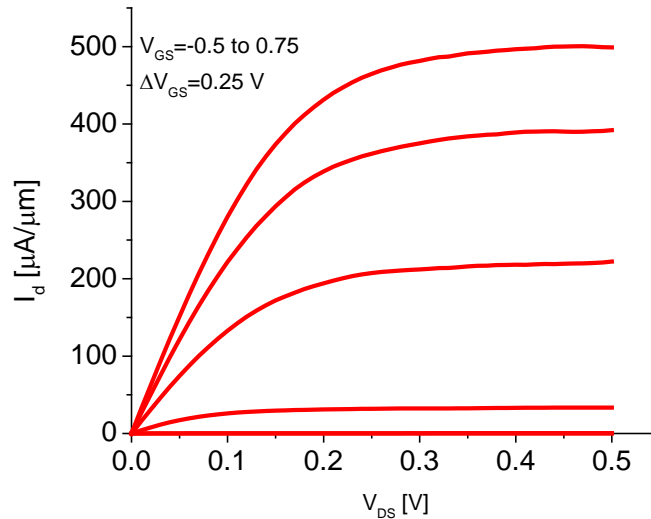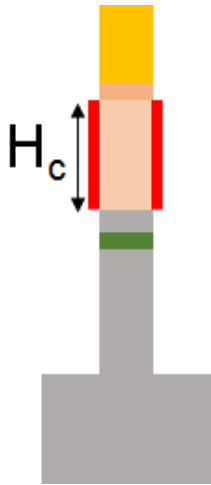
Current normalized by 2xH_c

At V_{DS}=0.5 V:

- g_m=900 µS/µm
- R_{on}=320 Ω·µm
- S_{sat}=100 mV/dec

Vardi, EDL 2016
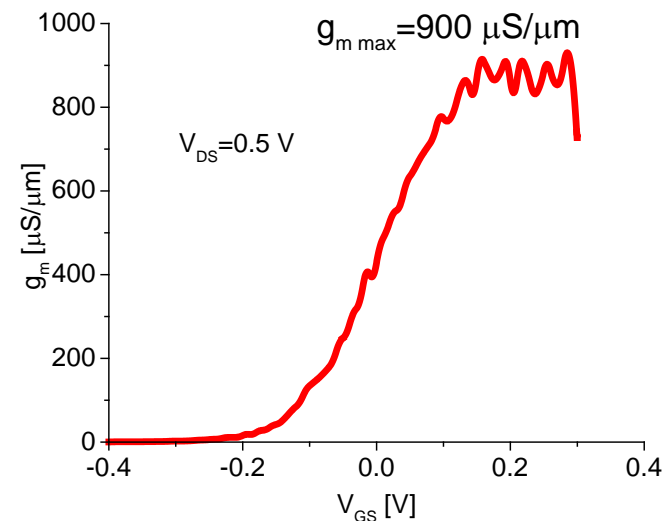
L_g and EOT scaling ($W_f \sim 20$ nm)

$V_{DS}=0.5$ V
$W_f=20\text{-}22$ nm

EOT↓

A: Al_2O_3, EOT=2.8 nm
B: Al_2O_3/HfO_2, EOT=1 nm
C: HfO_2, EOT=0.6 nm

60 mV/dec

EOT↓
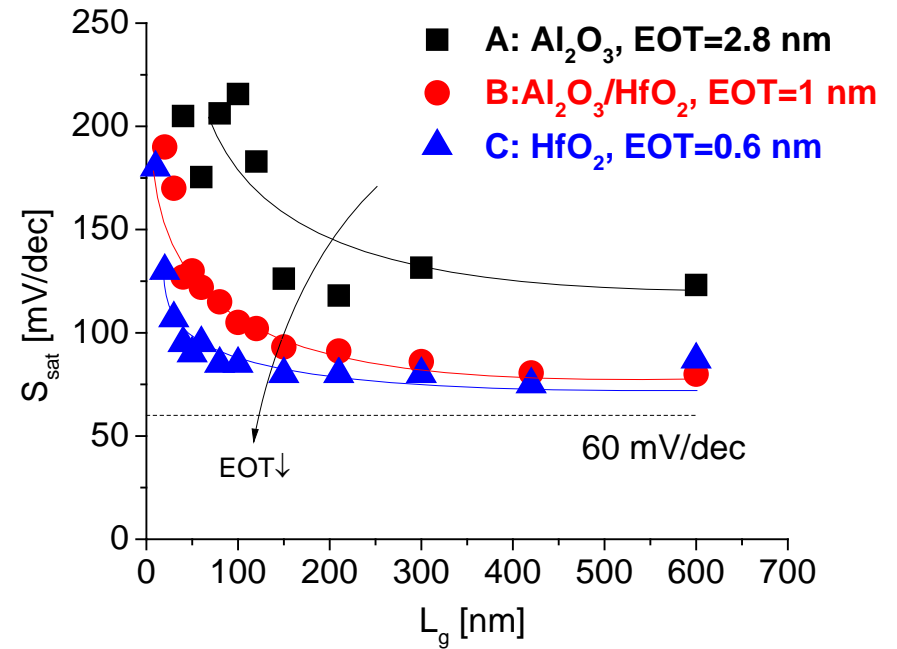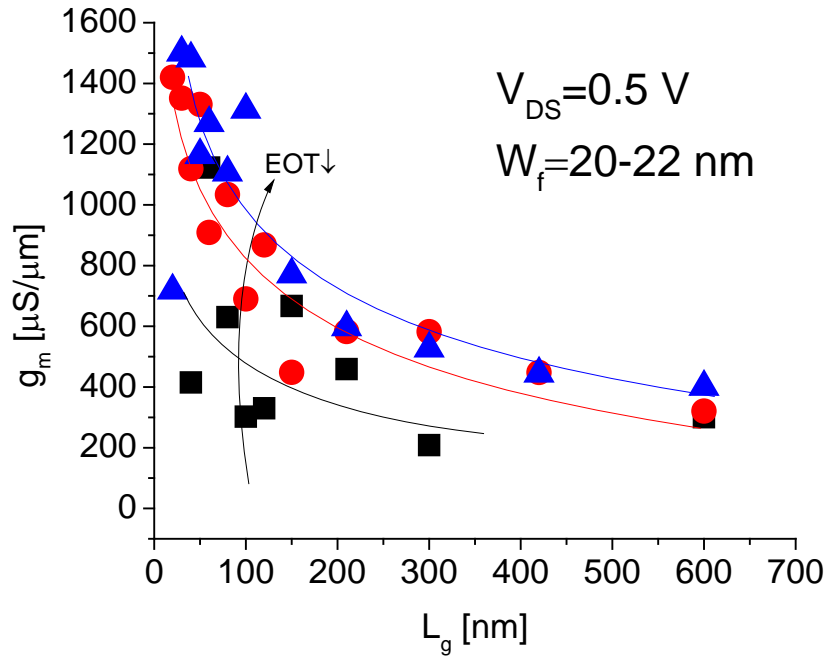
Classical scaling with L_g and EOT

Vardi, EDL 2016

Fin-width scaling (EOT=0.6 nm)

Left plot: $g_{m\,max}$ [μS/μm] vs L_g [nm], with curves labeled W_f=22 nm, ΔW_f= 5 nm, down to 7.

Right plot: $S_{sat,min}$ [mV/dec] vs L_g [nm].
Contaminated by gate leakage
60 mV/dec

- W_f=7 nm
- W_f=12 nm
- W_f=17 nm
- W_f=22 nm
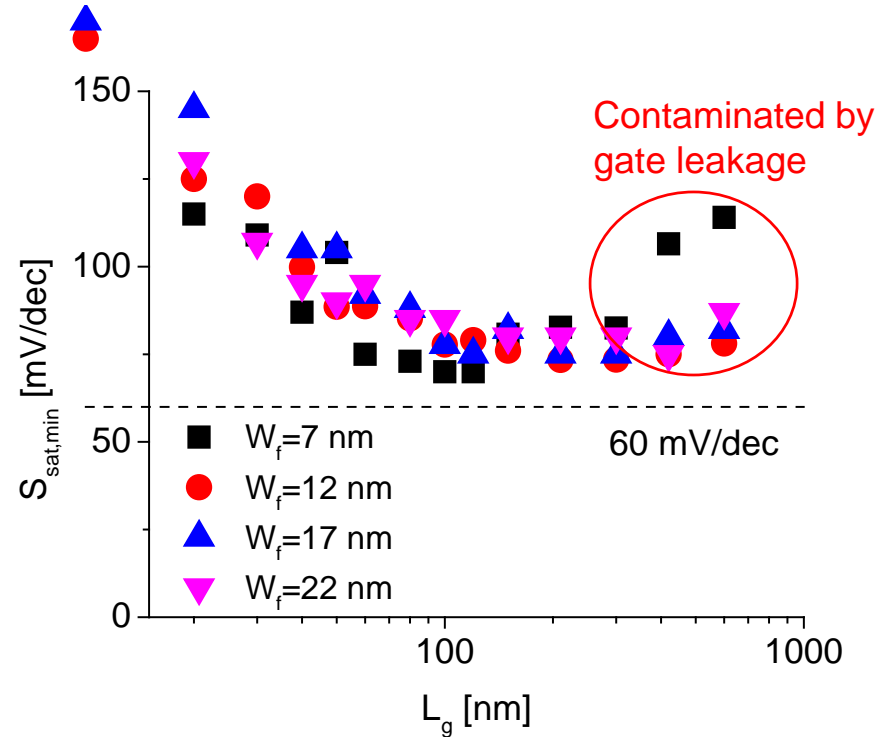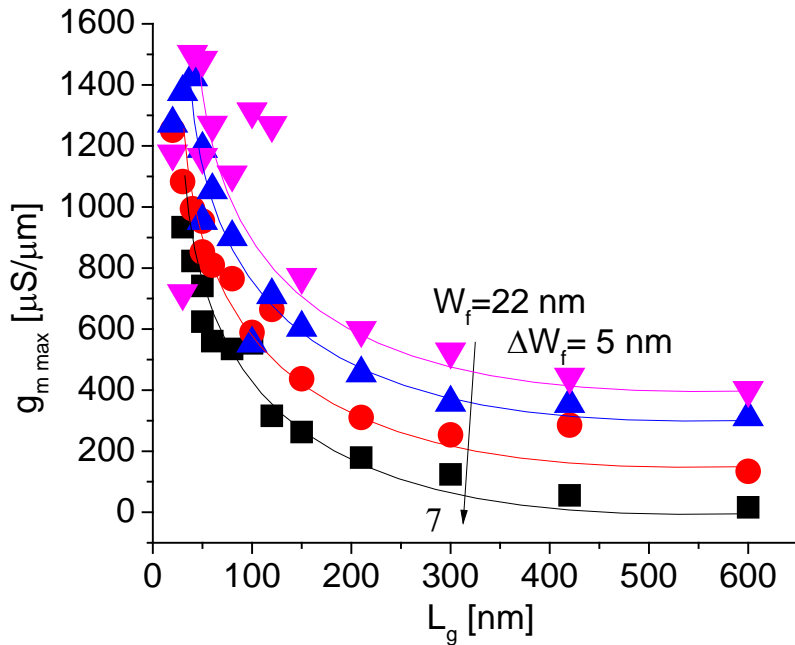
- **Non-ideal fin width scaling**
- **Sources:**
  - **High D_{it} (~5×10^{12} cm^{-2}.eV^{-1})?**
  - **mobility degradation?**
  - **line edge roughness?**

Vardi, EDL 2016

19

InGaAs FinFET benchmarking

g_m normalized by fin width
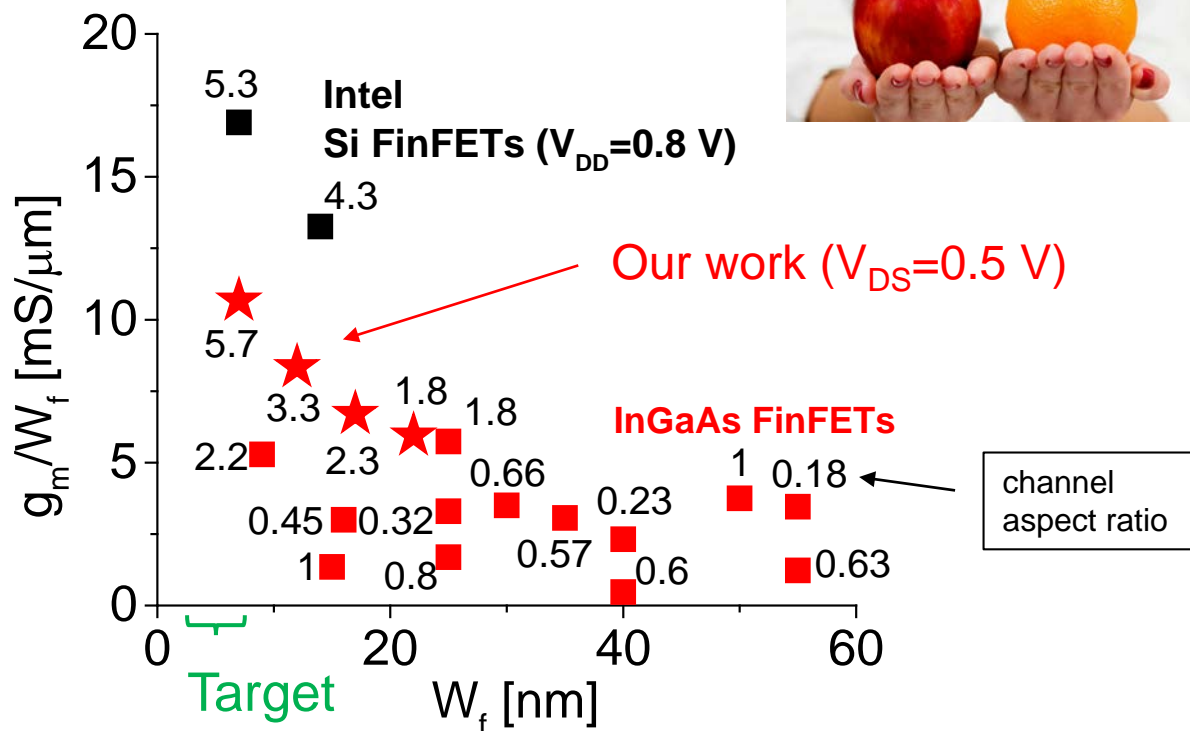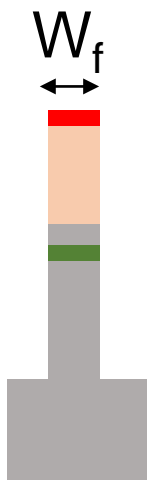
- First InGaAs FinFETs with $W_f < 10$ nm
- Doubled g_m over earlier InGaAs FinFETs
- Short of Si FinFETs → sidewall quality?

See latest at IEDM 2017!

InGaAs Vertical Nanowire MOSFETs

VNW MOSFET

Vertical nanowire MOSFET: ultimate scalable transistor

Vertical NW MOSFET:

→ uncouples footprint scaling from L_g, L_{spacer}, and L_c scaling

InGaAs Vertical Nanowires @ MIT

Key enabling technologies:
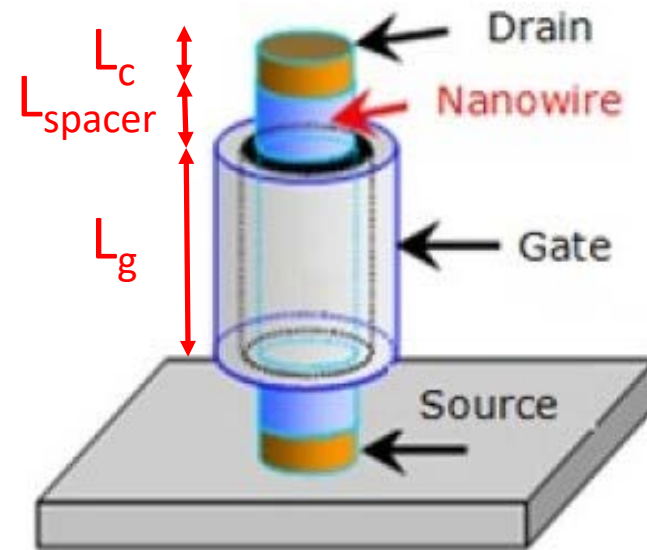
- RIE = $BCl_3/SiCl_4/Ar$ chemistry
- Digital Etch (DE) =

self-limiting O_2 plasma oxidation + H_2SO_4 or HCl oxide removal

- Radial etch rate=1 nm/cycle
- Sub-20 nm NW diameter
- Aspect ratio > 10
- Smooth sidewalls

Zhao, IEDM 2013
Zhao, EDL 2014
Zhao, IEDM 2014

RIE   + 5 cycles DE

240 nm — 28 nm

240 nm — 18 nm

23
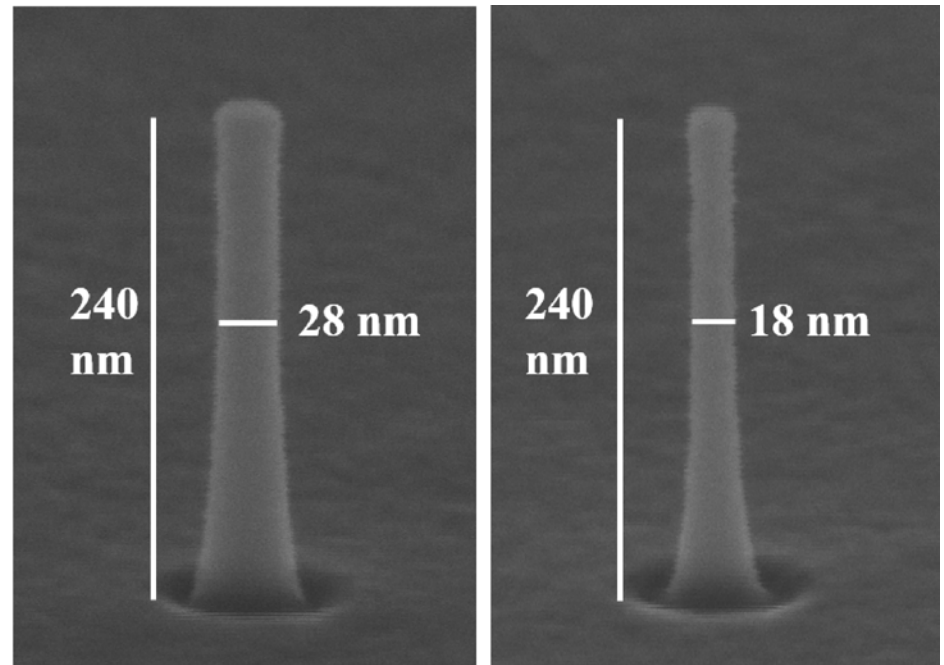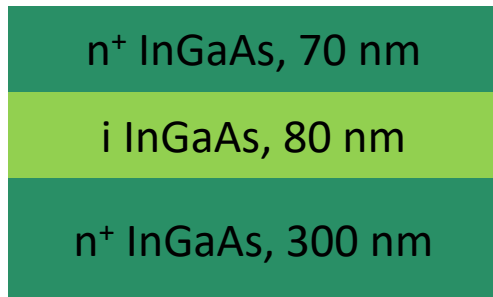
InGaAs VNW-MOSFETs
by top-down approach @ MIT

Starting heterostructure:

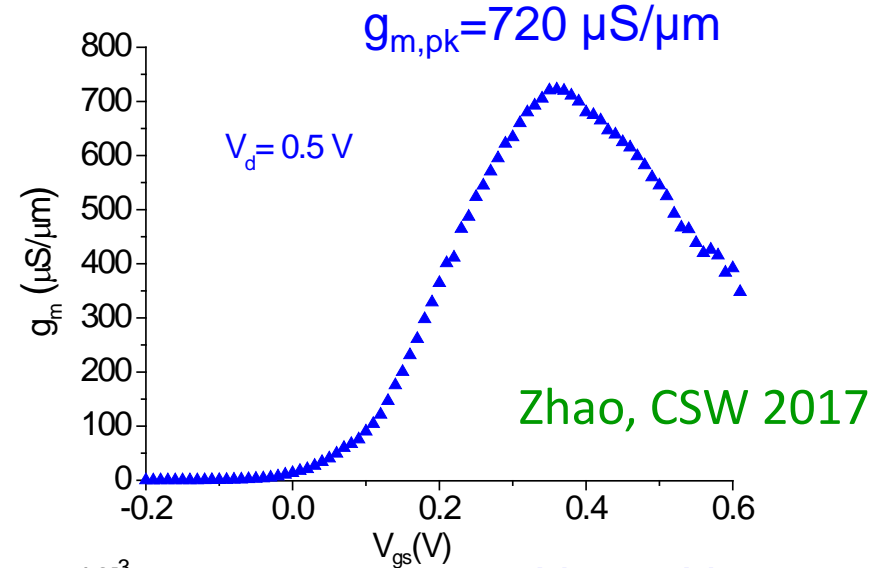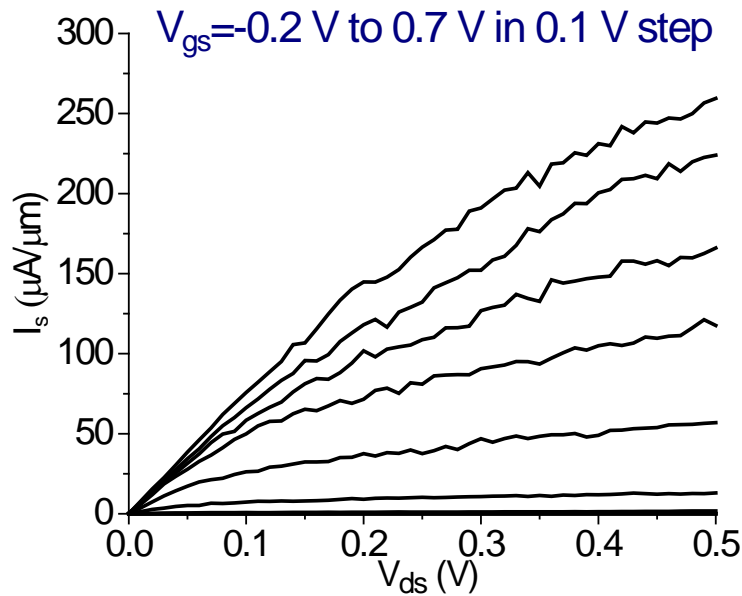| |
|---|
| n+ InGaAs, 70 nm |
| i InGaAs, 80 nm |
| n+ InGaAs, 300 nm |

n+: 6×10^{19} cm^{-3} Si doping
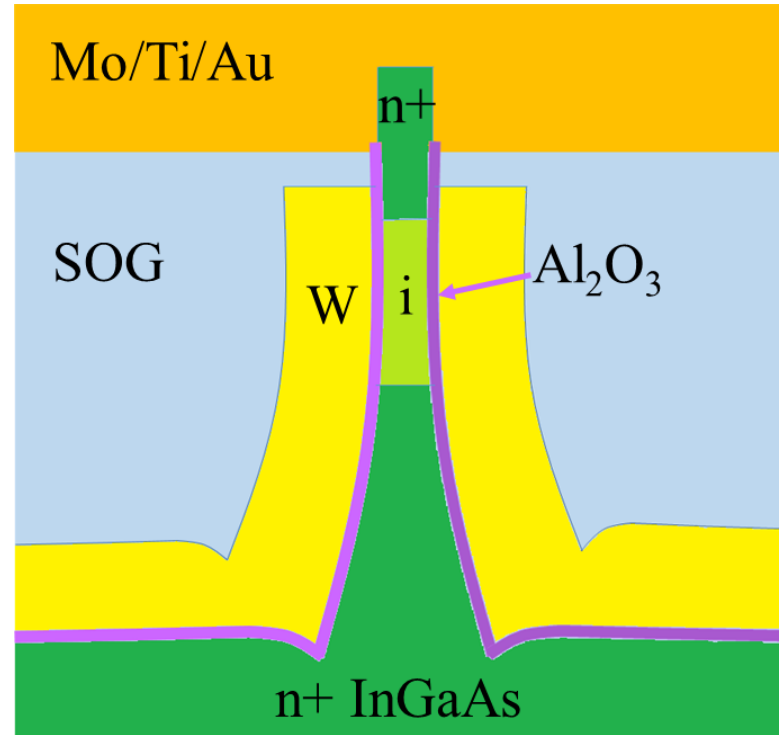
Top-down approach: flexible and manufacturable

VNW-MOSFET I-V characteristics: D=40 nm

V_{gs}=-0.2 V to 0.7 V in 0.1 V step

I_s (μA/μm) vs V_{ds} (V)

$g_{m,pk}$=720 μS/μm

V_d= 0.5 V

g_m (μS/μm) vs V_{gs}(V)

Zhao, CSW 2017

Single nanowire MOSFET:

- L_{ch}= 80 nm
- 3 nm Al_2O_3 (EOT = 1.5 nm)

V_{ds}=0.5 V

V_{ds}=0.05 V

I_s (A/μm) vs V_{gs}(V)

S_{lin} = 70 mV/dec
S_{sat} = 80 mV/dec
DIBL = 88 mV/V
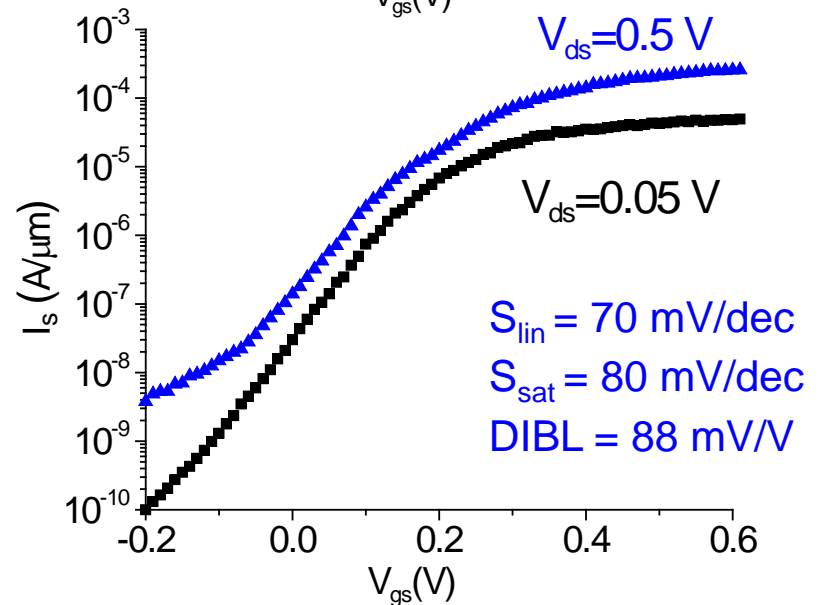
Benchmark with Si/Ge VNW MOSFETs

Peak g_m of InGaAs (V_{DS}=0.5 V), Si and Ge VNW MOSFETs
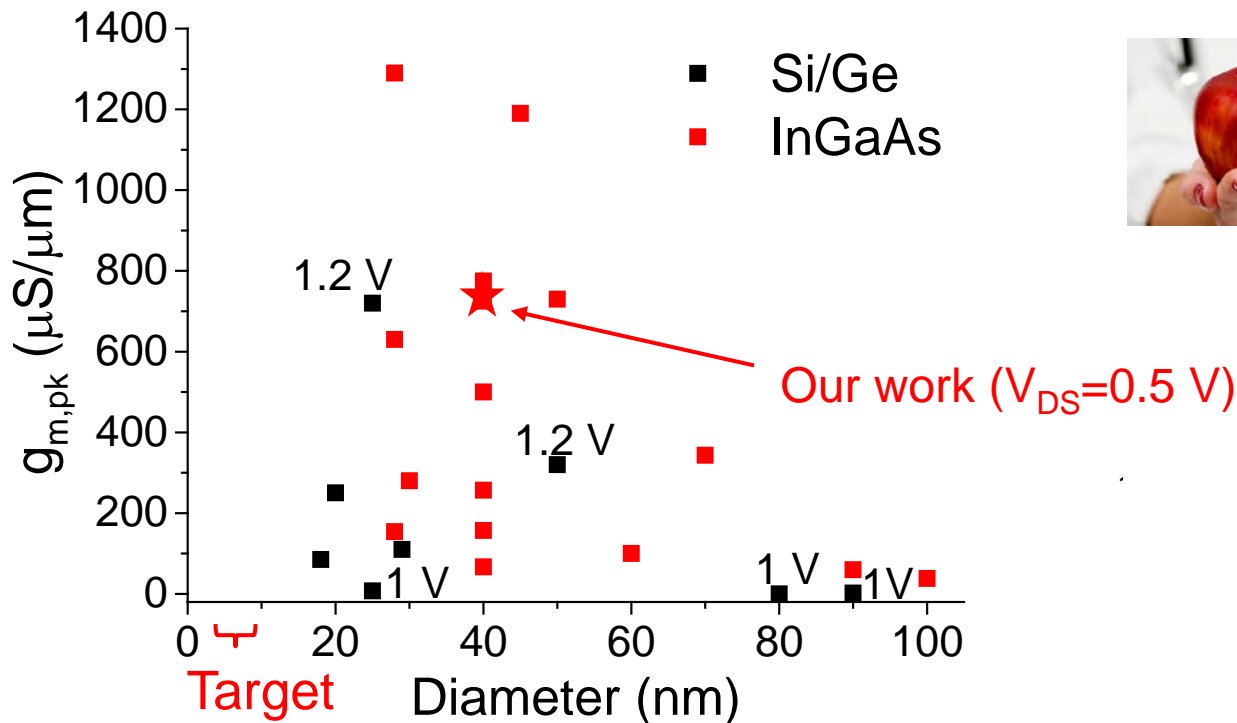
- InGaAs competitive with Si
- Need to demonstrate VNW MOSFETs with D<10 nm

InGaAs VNW Mechanical Stability for D<10 nm
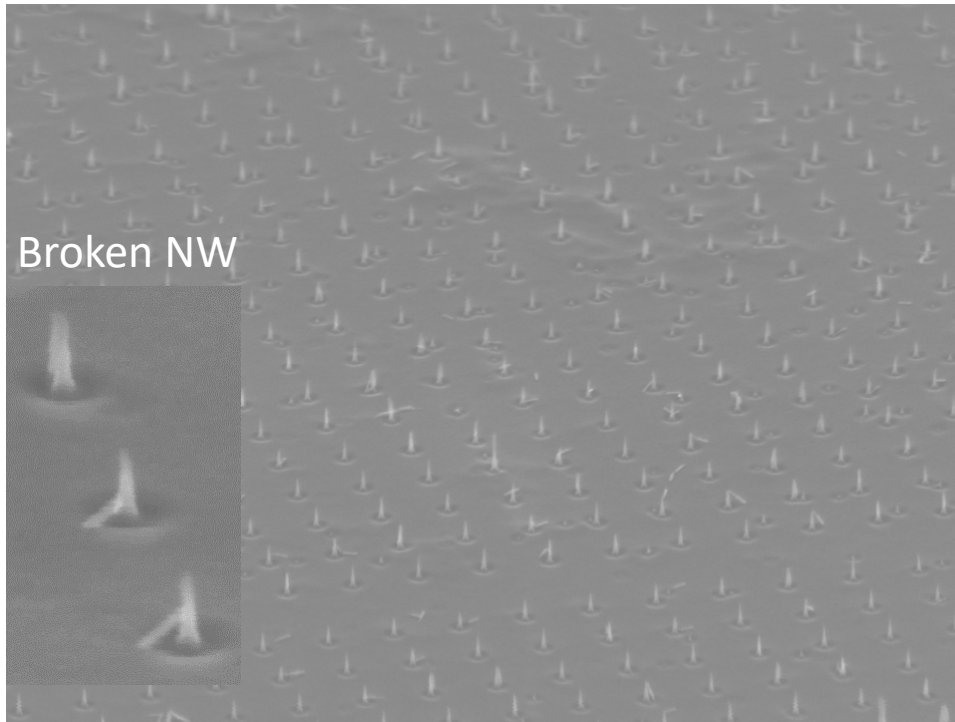
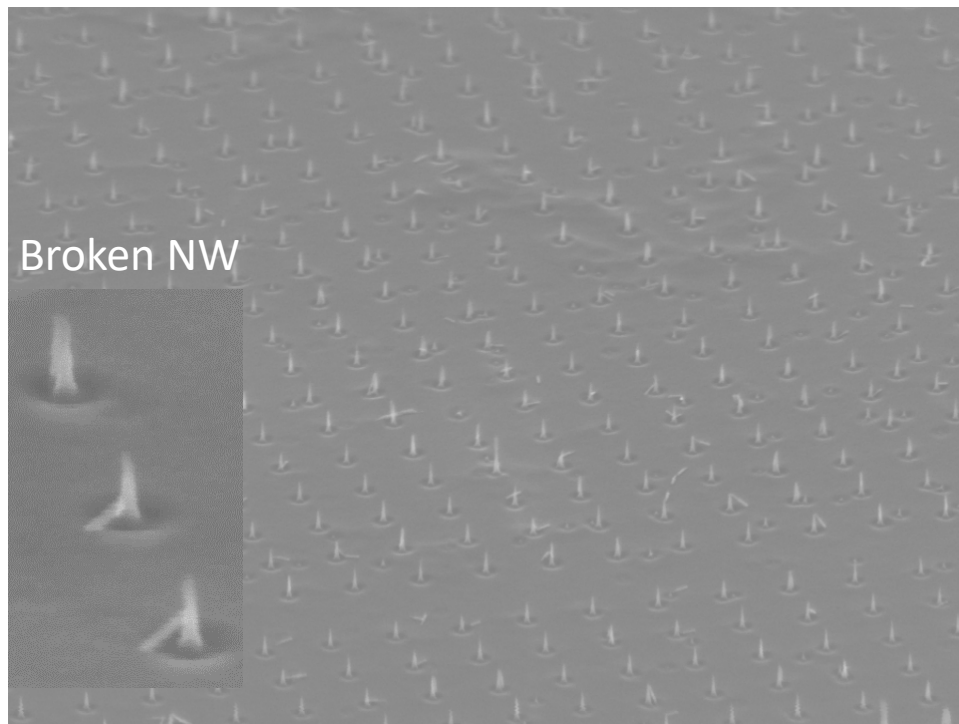8 nm InGaAs VNWs after 7 DE cycles:

Yield = 0%

Broken NW

Difficult to reach 10 nm VNW diameter due to breakage

InGaAs VNW Mechanical Stability for D<10 nm

Difficult to reach 10 nm VNW diameter due to breakage

Yield = 0%

Broken NW

Water-based acid is problem:

Surface tension (mN/m):

- Water: 72
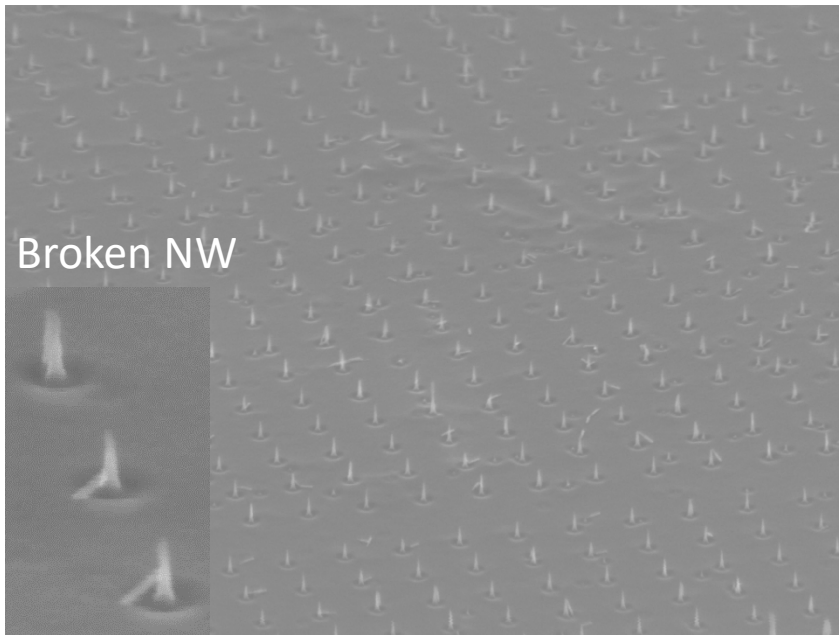- Methanol: 22
- IPA: 23

Solution: *alcohol-based digital etch*

Alcohol-Based Digital Etch
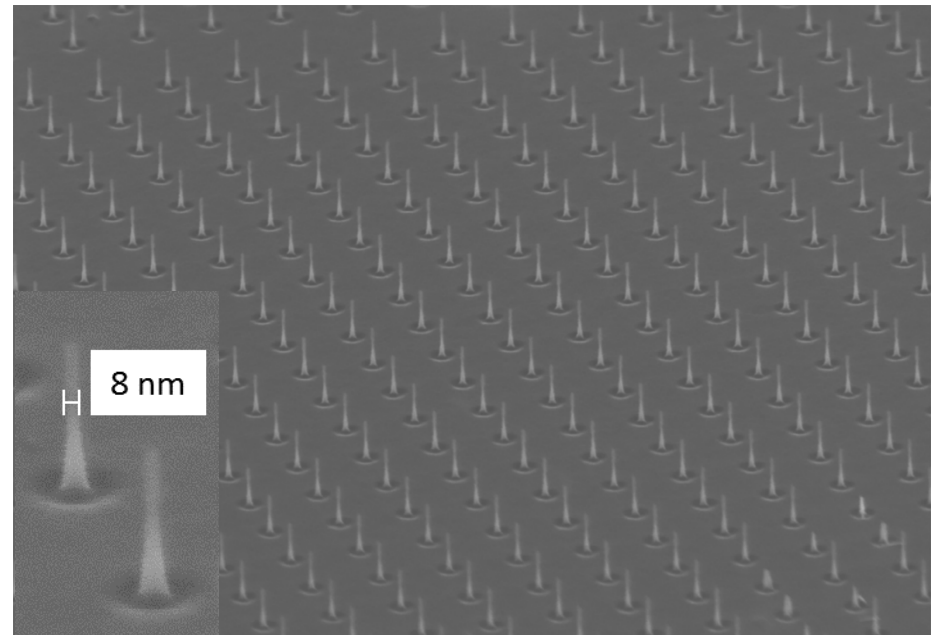
8 nm InGaAs VNWs after 7 DE cycles:

Lu, EDL 2017

10% HCl in DI water
Yield = 0%

10% HCl in IPA
Yield = 97%

Broken NW

H 8 nm

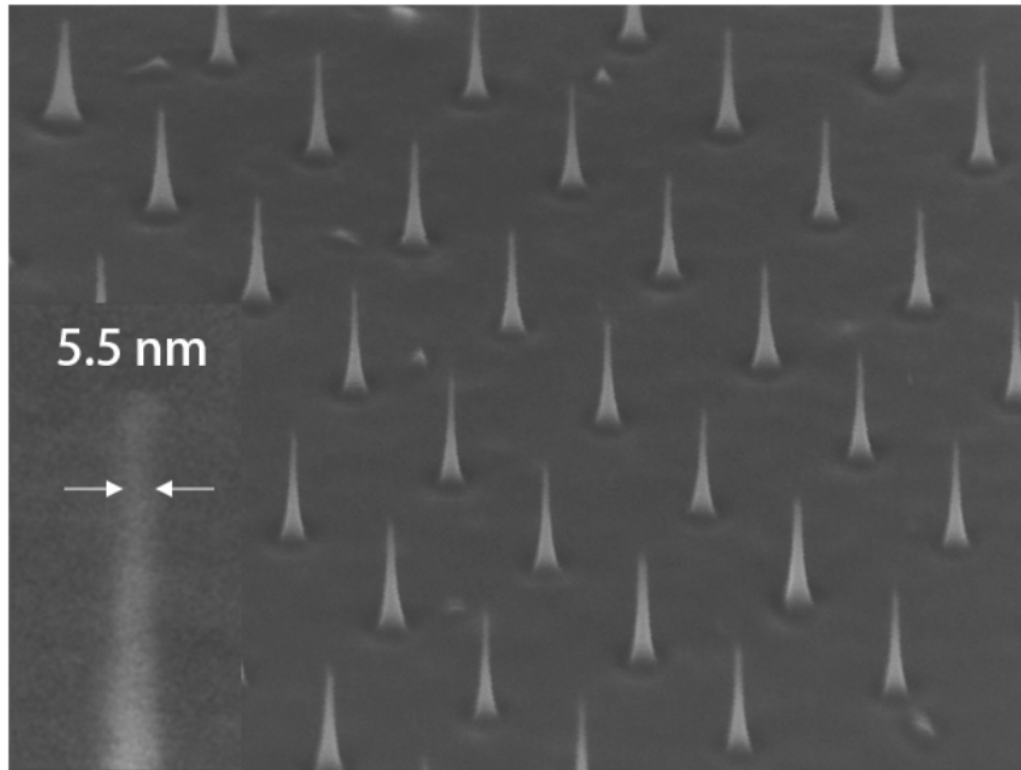Radial etch rate: 1.0 nm/cycle

Radial etch rate: 1.0 nm/cycle

Alcohol-based DE enables D < 10 nm
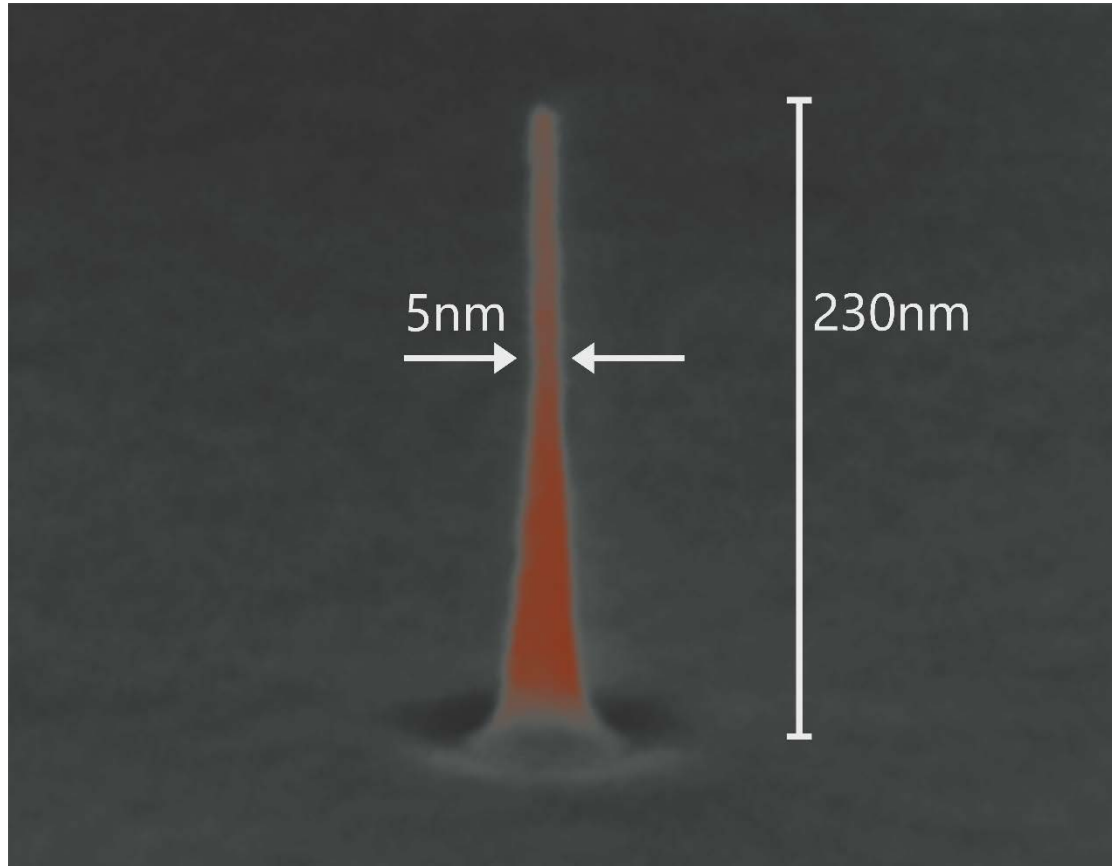
D=5.5 nm VNW arrays
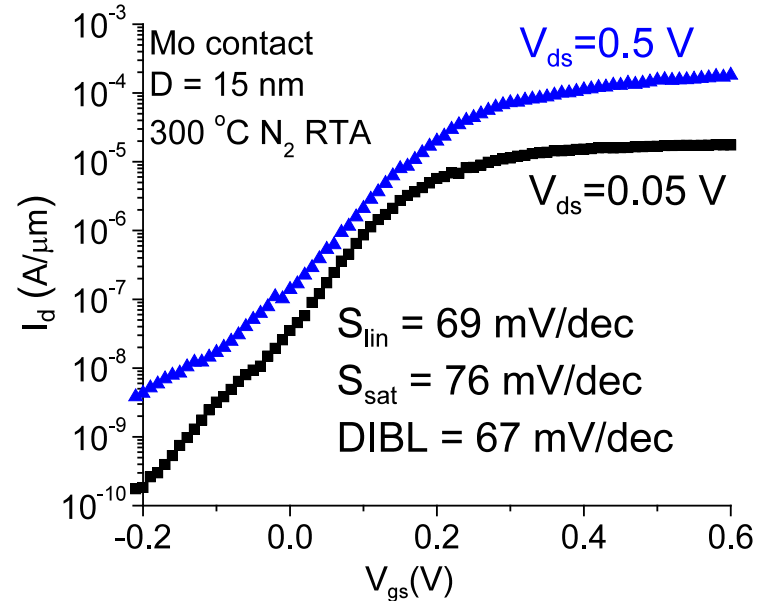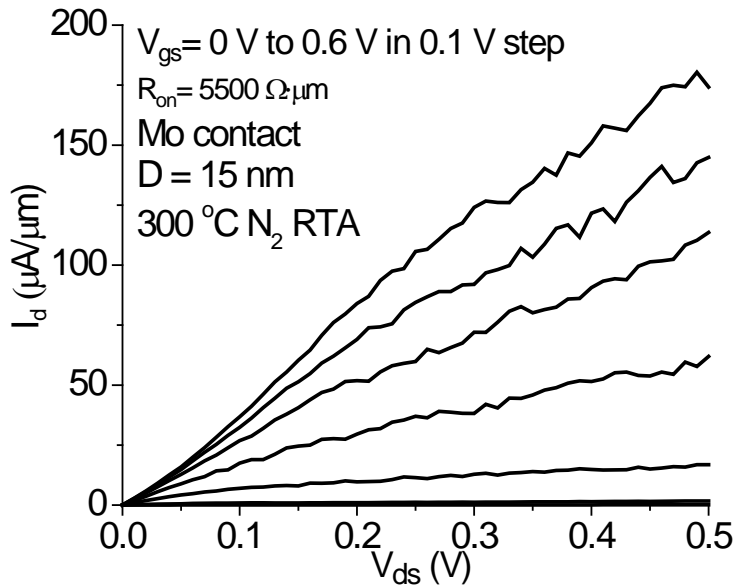
10% H_2SO_4 in methanol

90% yield

5.5 nm

- H_2SO_4:methanol yields 90% at D=5.5 nm!
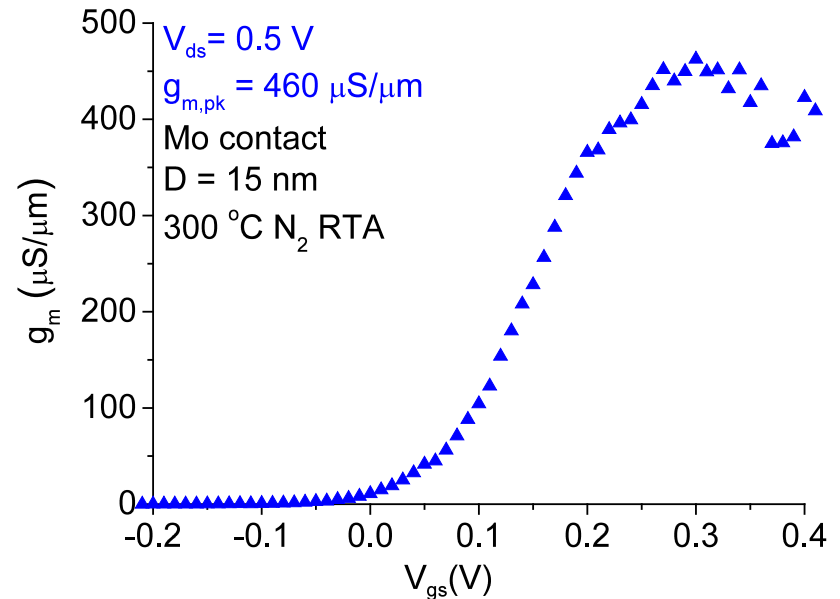- Viscosity matters: methanol (0.54 cP) vs. IPA (2.0 cP)

InGaAs Digital Etch

First demonstration of D=5 nm diameter InGaAs VNW
(Aspect Ratio > 40)

Latest! D=15 nm InGaAs VNW MOSFET

V_{gs}= 0 V to 0.6 V in 0.1 V step
R_{on}= 5500 $\Omega\cdot\mu m$
Mo contact
D = 15 nm
300 ^{o}C N_2 RTA

Mo contact
D = 15 nm
300 ^{o}C N_2 RTA

V_{ds}=0.5 V

V_{ds}=0.05 V

S_{lin} = 69 mV/dec
S_{sat} = 76 mV/dec
DIBL = 67 mV/dec

Single nanowire MOSFET:

- L_{ch}= 80 nm
- 2.5 nm Al_2O_3 (EOT = 1.3 nm)

V_{ds}= 0.5 V
$g_{m,pk}$ = 460 $\mu S/\mu m$
Mo contact
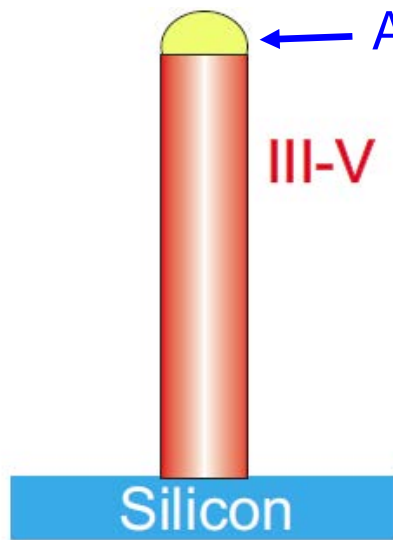D = 15 nm
300 ^{o}C N_2 RTA

Zhao, IEDM 2017

Benchmark with Si/Ge VNW MOSFETs

Peak g_m of InGaAs (V_{DS}=0.5 V), Si and Ge VNW MOSFETs
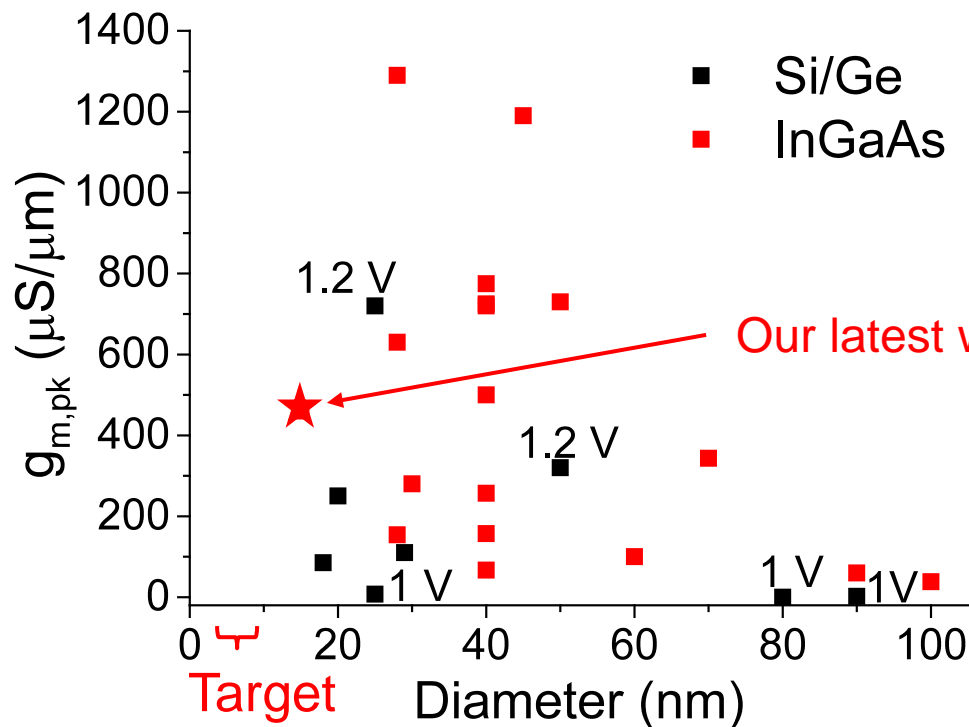
Most aggressively scaled VNW MOSFET ever
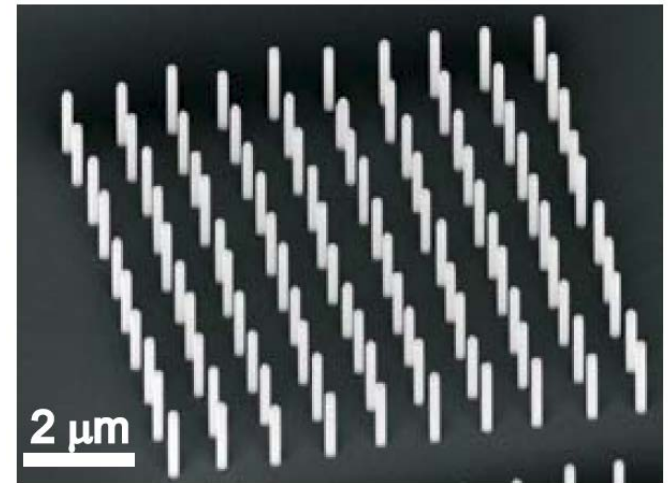
InGaAs Vertical Nanowires on Si by direct growth

← Au seed

III-V

Silicon

Vapor-Solid-Liquid (VLS) Technique
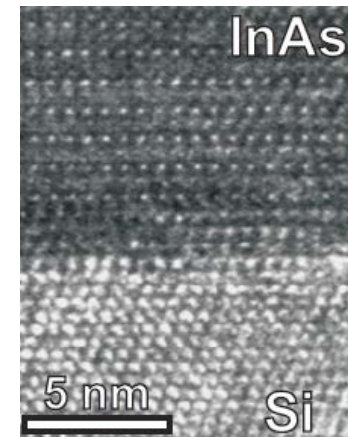

III-V

SiO$_2$

Silicon
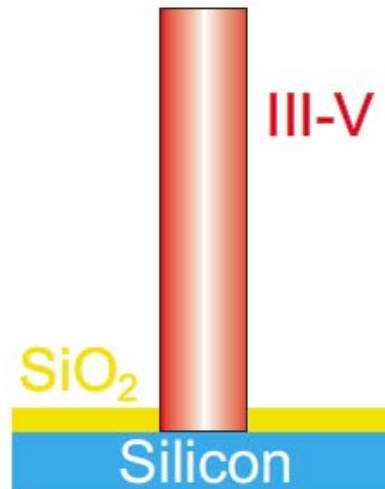
Selective-Area Epitaxy (SAE)

Riel, MRS Bull 2014

2 μm

InAs NWs on Si by SAE

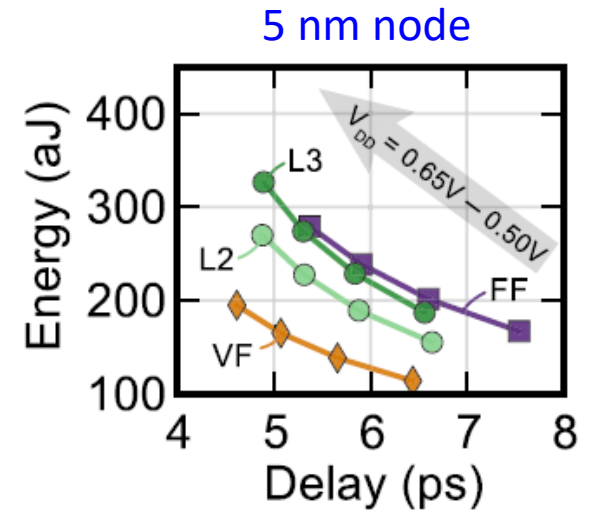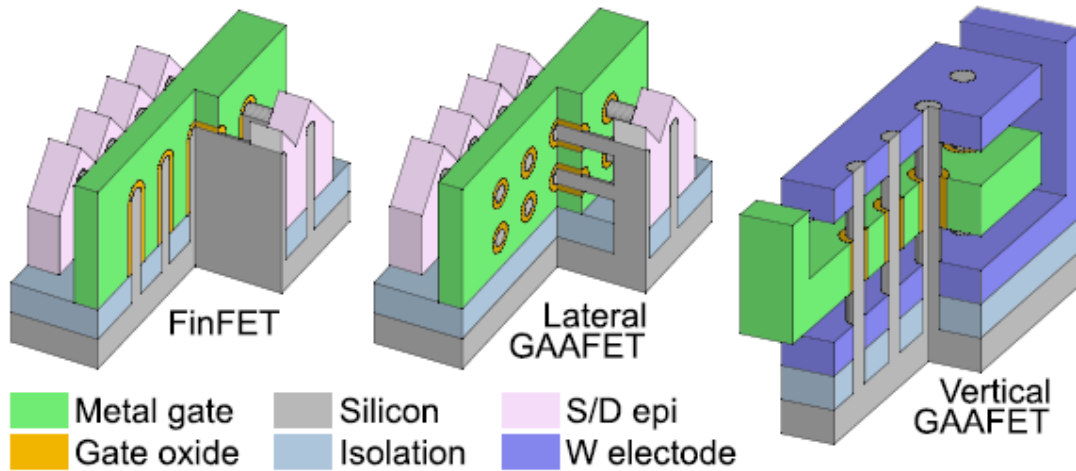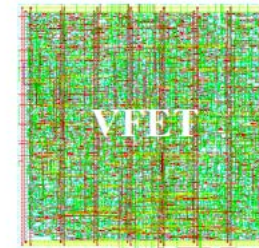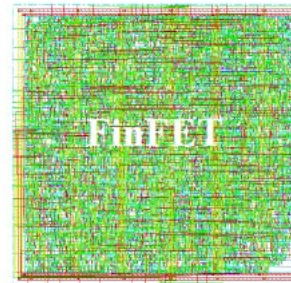
InAs

5 nm   Si

Riel, IEDM 2012

VNW MOSFETs: path for III-V integration on Si for future CMOS

Vertical nanowire MOSFET for 5 nm node

5 nm node

Yakimets, TED 2015
Bao, ESSDERC 2014

30% area reduction in 6T-SRAM
19% area reduction in 32 bit multiplier

Vertical NW:

→ power, performance and area gains w.r.t. Lateral NW or FinFET

Conclusions

1. Great recent progress on planar, fin and nanowire InGaAs MOSFETs

2. Device performance still lacking for 3D architecture designs

3. III-V Vertical-Nanowire MOSFETs: most likely architecture for future integration with Si

4. Many, MANY issues to work out:

   sub-10 nm fin/nanowire fabrication, self-aligned contacts, device asymmetry, introduction of mechanical stress, V_T control, sidewall roughness, device variability, BTBT and parasitic HBT gain, oxide trapping, self-heating, reliability, NW survivability, co-integration on n- and p-channel devices on Si, interface states, metal routing, contact resistance < 10^{-9} $\Omega.cm^{-2}$, off-state leakage, TDDB, etc....